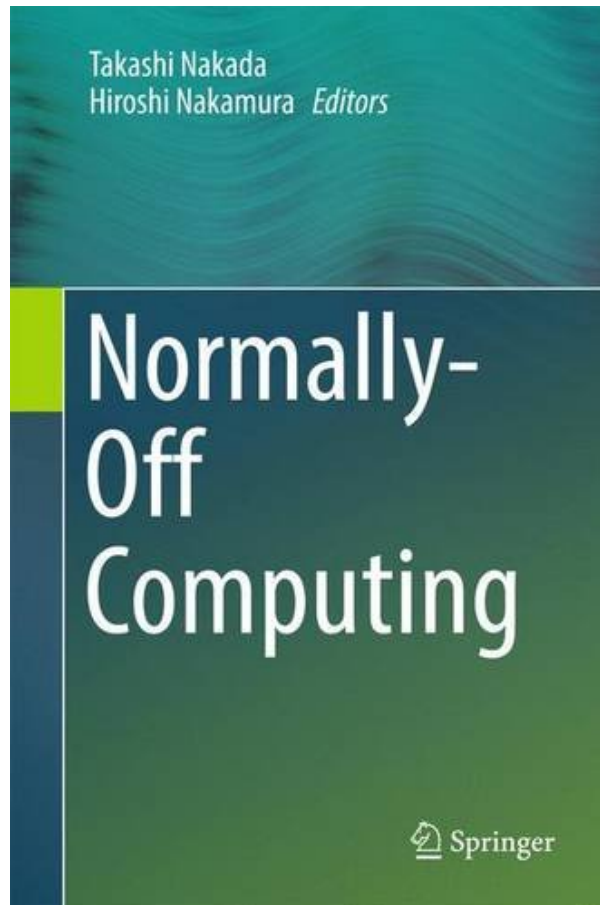


# NORMALLY-OFF COMPUTING FROM SPRINGER



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Takashi Nakada  
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# Normally- Off Computing

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## From the Back Cover

As a step toward ultimate low-power computing, this book introduces normally-off computing, which involves inactive components of computer systems being aggressively powered off with the help of new non-volatile memories (NVMs). Because the energy consumption of modern information devices strongly depends on both hardware and software, co-design and co-optimization of hardware and software are indispensable to improve energy efficiency.

The book discusses various topics including (1) details of low-power technologies including power gating, (2) characteristics of several new-generation NVMs, (3) normally-off computing architecture, (4) important technologies for implementing normally-off computing, (5) three practical implementations: healthcare, mobile information devices, and sensor network systems for smart city applications, and (6) related research and development.

Bridging computing methodology and emerging memory devices, the book is designed for both hardware and software designers, engineers, and developers as comprehensive material for understanding normally-off computing.

## About the Author

## About the Editors

Hiroshi Nakamura is a professor in the Department of Information Physics and Computing at The University of Tokyo. He is also the director of the Information Technology Center at The University of Tokyo. He received the Ph.D. degree in electrical engineering from The University of Tokyo in 1990.

His research interests are ultra-low-power VLSI design, power-aware computing systems, and high-performance parallel computer systems. He has been an executive committee member of the IEEE/ACM International Symposium on Low-Power Electronics and Design (ISLPED) since 2012 and a steering

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